IN THE CLAIMS

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
4. (Cancelled)
5. (Cancelled)
6. (Cancelled)
7. (Cancelled)
8. (Cancelled)
9. (Cancelled)

10. (Amended) An integrated circuit formed by a method comprising the steps of:~~according to the method of claim 1~~

recessing a first portion of a surface of a monolithic semiconducting substrate without effecting a second portion of the surface of the monolithic semiconducting substrate, by

growing a thermal oxide layer on the surface of the substrate,

depositing a nitride masking layer on the thermal oxide layer,

forming a patterning layer on the nitride masking layer,

forming openings in the patterning layer,

etching portions of the nitride masking layer and the thermal oxide layer through the openings in the patterning layer,

removing the patterning layer,

recessing the first portion of the surface of the substrate underlying the etched portions of the nitride masking layer and the thermal oxide layer, and

stripping off all material remaining on the surface of the substrate,

implanting an insulator precursor species of one of oxygen and nitrogen beneath the surface of the recessed first portion of the monolithic semiconducting substrate,

etching a trench around the implanted and recessed first portion of the monolithic semiconducting substrate,

activating the insulator precursor species to form an insulator layer beneath the surface of the recessed first portion of the monolithic semiconducting substrate, thereby elevating the surface of the recessed first portion of the substrate to be substantially planar with the second portion of the surface of the substrate,

forming a semiconductor on insulator structure in the first portion of the monolithic semiconducting substrate, and

forming a bulk semiconductor structure in the second portion of the monolithic semiconducting substrate.

11. (Cancelled)
12. (Cancelled)
13. (Cancelled)
14. (Cancelled)
15. (Cancelled)
16. (Cancelled)
17. (Cancelled)
18. (Cancelled)
19. (Cancelled)

20. (Original) A monolithic integrated circuit having a semiconductor on insulator circuit structure formed in a first portion of the substrate, the first portion of the substrate having a first surface and a semiconducting layer overlying an insulating layer that extends to a depth within the substrate, the first portion of the substrate surrounded by a filled trench that extends below the depth of the insulating layer of the first portion, the integrated circuit also having a bulk semiconducting circuit structure formed in a second portion of a substrate, the second portion of the substrate having a second surface, where the first surface is substantially coplanar with the second surface.